In the Claims:

Please cancel claims 7, 9, 11 and 21. Please amend claims 2-6 and 12-20. The claims are as follows:

1. (Canceled)

2. (Currently Amended) An electronic ~~circuit~~ device , comprising:

a self-timed memory cell array;

an address decode circuit connected through a wordline driver to wordlines of said self-timed memory cell array and to a sense amplifier self-timed decode circuit ~~adapted to set a base read time delay of said memory cell array~~; and

a read delay adjustment circuit including a sense amplifier delay circuit and a read margin adjustment circuit, said read margin circuit coupled to said sense amplifier delay circuit, an input of said sense amplifier delay circuit coupled to said sense amplifier self-timed decode circuit, an output of said sense amplifier delay circuit coupled to sense amplifiers on bitlines of said self-timed memory cell array through a sense amplifier driver, said read ~~delay~~ margin adjustment circuit ~~adapted to adjust said base read time delay of said memory array based on~~ responsive to an operating frequency of said ~~memory cell array~~ electronic device;

~~a sense amplifier delay circuit coupled between said sense amplifier self timed decode circuit and said memory cell array, said sense amplifier delay circuit adapted to control an amount of delay time added to said base read time delay in response to a margin select signal;~~

and

~~a read margin adjustment circuit coupled to said sense amplifier delay circuit, said read margin adjustment circuit adapted to generate said margin select signal~~.

3. (Currently Amended) The ~~circuit~~ device of claim 2, wherein said read margin adjustment circuit includes:

a microprocessor ~~adapted~~ including a load instruction register and a margin control register, said microprocessor responsive to ~~execute~~ a load instruction ~~issued in response to a change of value of said~~ stored in said load instruction register, said load instruction indicating an operating frequency of said microprocessor ~~and of said memory cell array and to store data associated with said load instruction in a~~, said load instruction register coupled to said margin control register, an output of said margin control register ~~coupled~~ connected to said sense amplifier delay circuit.

4. (Currently Amended) The ~~circuit~~ device of claim 2, wherein said read margin adjustment circuit includes:

a microprocessor ~~adapted~~ including a clock control unit and a frequency selector and a margin control register ~~to generate a frequency select signal to select an operating frequency of said microprocessor and said operating frequency of said memory cell array; and~~

, said clock control unit responsive to an operating frequency of said microprocessor, said clock control unit coupled to said frequency selector and to said margin control register

~~a register adapted to store said frequency select signal~~, an output of said margin control register coupled to said sense amplifier delay circuit.

5. (Currently Amended) The ~~circuit~~ device of claim 2, wherein said read margin adjustment circuit includes:

a frequency selection circuit ~~adapted to generate said operating frequency of said memory cell array from~~ coupled to an internal frequency generation circuit or ~~from~~ to an external clock signal; and

a frequency detector coupled between said frequency selection circuit and said sense amplifier delay circuit.

6. (Previously Presented) The ~~circuit~~ device of claim 2, further including one or more programmable fuses coupled to said sense amplifier delay circuit, said sense amplifier delay circuit ~~adapted to set an initial time adjustment to said base read time delay based on~~ responsive a state of said one or more fuses.

7 - 11 (Canceled)

12. (Currently Amended) A method ~~for adjusting the read margin of a self-timed memory cell array~~, comprising:

providing an electronic device, said electronic device including a self-timed memory cell array, an address decode circuit, a sense amplifier self-timed decode circuit and a read delay adjustment circuit, said read delay adjustment circuit including a sense amplifier delay circuit and a read margin adjustment circuit, said address decode circuit coupled through a word line driver to wordlines of said self-timed memory array and to said sense amplifier self-timed decode circuit, said read margin adjustment circuit connected to said sense amplifier delay

circuit, said sense amplifier delay circuit connected to said sense amplifier self-timed decode circuit, an output of said sense amplifier delay circuit coupled to through a sense amplifier driver to sense amplifiers coupled to bitlines of said self-timed memory array;

~~providing a sense amplifier self timed decode circuit for~~ setting a base read time delay of said self-timed memory cell array; and

~~providing a read delay adjustment circuit coupled to said memory cell array, said read delay adjustment circuit for~~ adjusting said base read time delay of said self-timed memory array based on an operating frequency of said ~~memory cell array~~ electronic device.

13. (Currently Amended) The method of claim 12, ~~wherein said read delay adjustment circuit includes~~ further comprising:

~~a sense amplifier delay circuit coupled between said sense amplifier self timed decode circuit and said memory cell array, said sense amplifier delay circuit for~~ controlling an amount of delay time added to said base read time delay in response to a margin select signal; ~~and~~

~~a read margin adjustment circuit coupled to said sense amplifier delay circuit, said read margin adjustment circuit for generating said margin select signal~~.

14. (Currently Amended) The method of claim 13, wherein said read margin adjustment circuit includes a microprocessor including a load instruction register coupled to a margin control register and further comprising:

~~a microprocessor for~~ executing a load instruction stored in said load instruction register issued in response to a change of value of ~~said~~ an operating frequency of said microprocessor ~~and of said memory cell array~~ and ~~for~~ storing data associated with said load instruction in [[a]]

said margin control register, an output of said margin control register coupled to said sense amplifier delay circuit; and

~~further including,~~ when said operating frequency is to be decreased, sequentially decreasing said operating frequency, issuing said margin select signal and decreasing said operating voltage in the order recited and when said operating frequency is to be increased, sequentially increasing said operating voltage, issuing said margin select signal and increasing said operating voltage in the order recited.

15. (Currently Amended) The method of claim 13, wherein said read margin adjustment circuit includes a microprocessor including a clock control circuit coupled to a frequency selector and a margin control register, an output of said margin control register coupled to said sense amplifier delay circuit and further including:

generating a frequency select signal for selecting an operating frequency of said microprocessor and ~~said operating frequency~~ of said self-timed memory cell array;

~~a register for~~ storing said frequency select signal in said margin control register, ~~an output of said margin control register coupled to said sense amplifier delay circuit~~; and

~~further including,~~ when said operating frequency is to be decreased, sequentially decreasing said operating frequency, issuing said margin select signal and decreasing said operating voltage in the order recited and when said operating frequency is to be increased, sequentially increasing said operating voltage, issuing said margin select signal and increasing said operating voltage in the order recited.

16. (Currently Amended) The method of claim 13, wherein said read margin adjustment circuit includes a frequency selection circuit and a frequency detector coupled between said frequency selection circuit and said sense amplifier delay circuit and further comprising:

generating said operating frequency ~~of said memory cell array~~ from an internal frequency generation circuit or from an external clock signal~~; and~~

~~a frequency detector coupled between said frequency selection circuit and said sense amplifier delay circuit.~~

17. (Currently Amended) The method of claim 13, wherein said electron device further ~~including~~ includes one or more programmable fuses coupled to said sense amplifier delay circuit and further comprising:

~~providing one or more programmable fuses coupled to said sense amplifier delay circuit;~~ ~~said sense amplifier delay circuit for~~ setting an initial time adjustment to said base read time delay based on a state of said one or more fuses.

18. (Currently Amended) The method of claim 17, ~~wherein said sense amplifier delay circuit is adapted to~~ further comprising:

~~override~~ overriding said initial time adjustment based on said margin select signal.

19. (Currently Amended) The method of claim 12, ~~further including;~~

~~providing a microprocessor; and~~

wherein said memory cell array is a cache memory coupled to said microprocessor.

20. (Currently Amended) The method of claim 12, wherein said base read time delay is based on a first operating frequency and a corresponding first operating voltage, and ~~time adjustment to~~ adjusting said base read time delay is based on a second operating frequency and a corresponding second operating voltage.

21. (Canceled)